FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200301825-6	10/769,824	
APPLICANT		
Luiz Andre Barroso et al.		
FILING DATE	GROUP	
02-02-2004	2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
𝒵	1A	5,386,547	01-31-95	Jouppi	
	1B	5,778,437	07-07-98	Baylor et al.	
	1C	6,295,598	09-25-01	Beroni et al.	
	1D	6,202,127	03-13-01	Dean et al.	
	1E	5,457,679	10-10-95	Eng et al.	
	1F	5,440,752	08-08-95	Lentz et al.	
	1G	6,457,100	09-24-02	Ignatowski et al.	
	1H	6,263,405	07-17-01	Irie et al.	
	1I	5,634,110	05-27-97	Laudon et al.	
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)
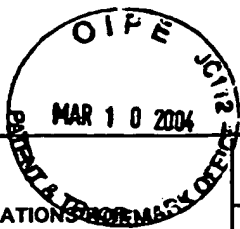
𝒵	1Q	Agrawal, Anant, et al., "An Evaluation of Directory Schemes for Cache Coherence", Proceedings of 15th International Symposium on Computer Architecture ("ISCA") (May 1998) pp. 280-289
𝒵	1R	Barroso, Luiz Andre, et al., "Impact of Chip-Level Integration on Performance of OLTP Workloads", High-Performance Computer Architecture ("HPCA") (January 2000)
𝒵	1S	Barroso, Luiz Andre, et al., "Memory System Characterization of Commercial Workloads", ISCA (June 1998)

EXAMINER	DATE CONSIDERED
Zhuo Li	02/17/05

Rev 10/03 (PTO1449)

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200301825-6	10/769,824	
APPLICANT		
Luiz Andre Barroso et al.		
FILING DATE	GROUP	
02-02-2004	2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A				
	2B				
	2C				
	2D				
	2E				
	2F				
	2G				
	2H				
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

ᴊᶜ	2Q	Eggers, Susan J., et al., "Simulation Multithreading: A Platform for Next-generation Processors", University of Washington, DEC Western Research Laboratory ((eggers.levyjlo)@cs.washington.edu) ((emer.stamm)@vssad.enet.dec.com) pp. 1-15 (1997)
ᴊᶜ	2R	Eickemeyer, Richard J., et al., "Evaluation of Multithreaded Uniprocessors for Commercial Application Environments", ACM (1996) (0-89791-786-3) pp. 203-213
ᴊᶜ	2S	Gupta, Anoop, et al., "Reducing Memory and Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes", Stanford University, Computer Systems Laboratory, pp 1-10 (1990)

EXAMINER   _Zuo Li._   DATE CONSIDERED   _02/17/05_

Rev 10/03 (PTO1449)

OTPE

MAR 1 0 2004

FORM PTO-1449	ATTY. DOCKET NO. 200301825-6	APPLICATION NO. 10/769,824	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT Luiz Andre Barroso et al.		
(Use several sheets if necessary)	FILING DATE 02-02-2004	GROUP 2186	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

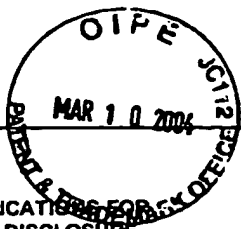|		
✗	3Q	Hammond, Lance, et al., "A Single-Chip Multiprocessor", IEEE (September 1997) (0018-9162)
✗	3R	Hammond, Lance, et al., "Data Speculation Support for a Chip Multiprocessor", Stanford University, Computer Systems Laboratory (http://www.hydra.stanford.edu/), (October 1998)
✗	3S	Jouppi, Norman P., et al., "Tradeoffs in Two-Level On-Chip Caching", WRL Research Report 93/3, Western Research Laboratory (WRL-Techreports@decwri.dec.com) (December 1993) pp. 1-31

EXAMINER Zhuo Li.	DATE CONSIDERED 02/17/05

FORM PTO-1449	ATTY. DOCKET NO. 200301825-6	APPLICATION NO. 10/769,824	CONFIRMATION NO.

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

APPLICANT Luiz Andre Barroso et al.	
FILING DATE 02-02-2004	GROUP 2186

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	4A				
	4B				
	4C				
	4D				
	4E				
	4F				
	4G				
	4H				
	4I				
	4J				
	4K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	4L					
	4M					
	4N					
	4O					
	4P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)
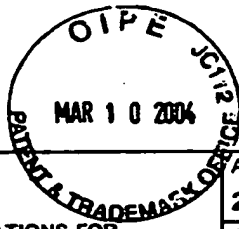
✓	4Q	Krishnan, Venkata, et al., "Hardware and Software Support for Speculative Execution of Sequential Binaries on a Chip-Multiprocessor", University of Illinois at Urbana-Champaign (http://iacoma.cs.uiuc.edu) (1998)
✓	4R	Kuskin, Jeffrey, et al., "The Stanford FLASH Multiprocessor", Stanford University, Computer Systems Laboratory (June 6, 1996)
✓	4S	Laudon, James, et al., "The SGI Origin: A ccNUMA Highly Scalable Server", Silicon Graphics, Inc. (laudon@sgi.com) (June 1997)

EXAMINER Zhuo Li	DATE CONSIDERED 02/17/05

Rev 10/03 (PTO1449)

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200301825-6	10/769,824	
APPLICANT		
Luiz Andre Barroso et al.		
FILING DATE	GROUP	
02-02-2004	2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	5A				
	5B				
	5C				
	5D				
	5E				
	5F				
	5G				
	5H				
	5I				
	5J				
	5K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	5L					
	5M					
	5N					
	5O					
	5P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)
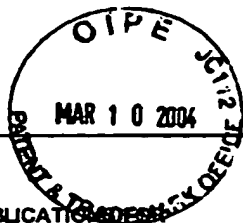
✗	5Q	Lenoski, Daniel et al., "The Directory-Based Cache Coherence Protcol for the DASH Multiprocessor", IEEE (1990) (CH2887-8) pp. 148-159
✗	5R	Nayfeh, Basem A., et al., "Evaluation of Design Alternatives for a Multiprocessor Microprocessor", ACM (1996) (0-89791-786-3) pp. 67-77
✗	5S	Nowatzyk, Andreas G., et al., "S-Connect: from Networks of Workstations to Supercomputer Performance", 22nd Annual International Symposium on Computer Architecture ("ISCA") (June 1995)

EXAMINER	DATE CONSIDERED
Zhuo Li	02/18/05

Rev 10/03 (PTO1449)

FORM PTO-1449	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
	200301825-6	10/769,824	
LIST OF PATENTS AND PUBLICATIONS IN APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT		
	Luiz Andre Barroso et al.		
	FILING DATE	GROUP	
(Use several sheets if necessary)	02-02-2004	2186	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	6A				
	6B				
	6C				
	6D				
	6E				
	6F				
	6G				
	6H				
	6I				
	6J				
	6K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	6L					
	6M					
	6N					
	6O					
	6P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

乙	6Q	Nowatzyk, Andreas, et al., "Exploiting Parallelism in Cache Coherency Protocol Engines", Sun Microsystems Computer Corporation (August 1995)
乙	6R	Olukotun, Kunle, et al., "The Case of a Single-Chip Multiprocessor", Proceedings Seventh International Symposium Architectural Support for Programming Languages and Operating Systems ("ASPLOS VII") (October 1996)
乙	6S	Steffan, J. Gregory, et al., "The Potential for Using Thread-Level Data Speculation to Facilitate Automatic Parallelization", HPCA-4 (February 1998) pp. 1-12

EXAMINER	DATE CONSIDERED
	02/18/05

Rev 10/03 (PTO1449)

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200301825-6	10/769,824	
APPLICANT		
Luiz Andre Barroso et al.		
FILING DATE	GROUP	
02-02-2004	2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	7A				
	7B				
	7C				
	7D				
	7E				
	7F				
	7G				
	7H				
	7I				
	7J				
	7K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	7L					
	7M					
	7N					
	7O					
	7P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)
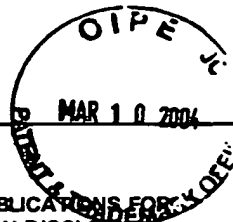
⁊ℓ	7Q	Tremblay, Marc, "MAJC-TM-5200 AVLIW Convergent MPSOC", Sun Microsystems, Inc., Microprocessor Forum (1999)
⁊ℓ	7R	Kunkel, Steven, et al., "System Optimization for OLTP Workloads, IEEE (1999) (0272-1732) pp. 56-64
⁊ℓ	7S	Diefendorff, Keith, "Power4 Focuses on Memory Bandwidth", Microdesign Resources, Microprocessor Report Vol. 13, No. 13, October 6, 1999

EXAMINER	DATE CONSIDERED
Zhuo Li	02/18/05

Rev 10/03 (PTO1449)

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200301825-6	10/769,824	
APPLICANT		
Luiz Andre Barroso et al.		
FILING DATE	GROUP	
02-02-2004	2186	

REFERENCE DESIGNATION   **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	8A				
	8B				
	8C				
	8D				
	8E				
	8F				
	8G				
	8H				
	8I				
	8J				
	8K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	8L					
	8M					
	8N					
	8O					
	8P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	8Q	Hammond, Lance, et al., "The Stanford Hydra CMP", Stanford University, Computer Systems Laboratory (http://www-hydra.stanford.edu) (March 2000), In EEE Micro, V.20 No. 2,
	8R	
	8S	

EXAMINER	DATE CONSIDERED
Zhuo Li.	02/18/05

Rev 10/03 (PTO1449)

FORM PTO-1449	ATTY. DOCKET NO. 200301825-6	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Luiz Andre Barroso et al.		
	FILING DATE Herewith	GROUP 2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,386,547	01-31-95	Jouppi	
	1B	5,778,437	07-07-98	Baylor et al.	
	1C	6,295,598	09-25-01	Beroni et al.	
	1D	6,202,127	03-13-01	Dean et al.	
	1E	5,457,679	10-10-95	Eng et al.	
	1F	5,440,752	08-08-95	Lentz et al.	
	1G	6,457,100	09-24-02	Ignatowski et al.	
	1H	6,263,405	07-17-01	Irie et al.	
	1I	5,634,110	05-27-97	Laudon et al.	
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Agrawal, Anant, et al., "An Evaluation of Directory Schemes for Cache Coherence", Proceedings of 15th International Symposium on Computer Architecture ("ISCA") (May 1998) pp. 280-289
	1R	Barroso, Luiz Andre, et al., "Impact of Chip-Level Integration on Performance of OLTP Workloads", High-Performance Computer Architecture ("HPCA") (January 2000)
	1S	Barroso, Luiz Andre, et al., "Memory System Characterization of Commercial Workloads", ISCA (June 1998)

EXAMINER Zhuo Li.	DATE CONSIDERED Feb. 17. 2005.

Rev 10/03 (PTO1449)

FORM PTO-1449	ATTY. DOCKET NO. 200301825-6	APPLICATION NO.	CONFIRMATION NO.

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

APPLICANT Luiz Andre Barr so et al.		
FILING DATE Herewith	GROUP 2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A				
	2B				
	2C				
	2D				
	2E				
	2F				
	2G				
	2H				
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

𝓎𝓁	2Q	Eggers, Susan J., et al., "Simulation Multithreading: A Platform for Next-generation Processors", University of Washington, DEC Western Research Laboratory ((eggers.levyjlo)@cs.washington.edu) ((emer.stamm)@vssad.enet.dec.com) pp. 1-15 (1997)
𝓎𝓁	2R	Eickemeyer, Richard J., et al., "Evaluation of Multithreaded Uniprocessors for Commercial Application Environments", ACM (1996) (0-89791-786-3) pp. 203-213
𝓎𝓁	2S	Gupta, Anoop, et al., "Reducing Memory and Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes", Stanford University, Computer Systems Laboratory, pp 1-10 (1990)

EXAMINER Zhuo Li.	DATE CONSIDERED Feb. 17. 2005

Rev 10/03 (PTO1449)

FORM PTO-1449	ATTY. DOCKET NO. 200301825-6		APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT Luiz Andre Barroso et al.			
(Use several sheets if necessary)	FILING DATE Herewith		GROUP 2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

⟋	3Q	Hammond, Lance, et al., "A Single-Chip Multiprocessor", IEEE (September 1997) (0018-9162)
⟋	3R	Hammond, Lance, et al., "Data Speculation Support for a Chip Multiprocessor", Stanford University, Computer Systems Laboratory (http://www.hydra.stanford.edu/), (October 1998)
⟋	3S	Jouppi, Norman P., et al., "Tradeoffs in Two-Level On-Chip Caching", WRL Research Report 93/3, Western Research Laboratory (WRL-Techreports@decwri.dec.com) (December 1993) pp. 1-31

EXAMINER Zhuo Li.	DATE CONSIDERED Feb. 17, 2004

Rev 10/03 (PTO1449)

FORM PTO-1449	ATTY. DOCKET NO. 200301825-6	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT Luiz Andre Barr so et al.		
(Use several sheets if necessary)	FILING DATE Herewith	GROUP 2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	4A				
	4B				
	4C				
	4D				
	4E				
	4F				
	4G				
	4H				
	4I				
	4J				
	4K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	4L					
	4M					
	4N					
	4O					
	4P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

✗	4Q	Krishnan, Venkata, et al., "Hardware and Software Support for Speculative Execution of Sequential Binaries on a Chip-Multiprocessor", University of Illinois at Urbana-Champaign (http://iacoma.cs.uiuc.edu) (1998)
✗	4R	Kuskin, Jeffrey, et al., "The Stanford FLASH Multiprocessor", Stanford University, Computer Systems Laboratory (June 6, 1996)
✗	4S	Laudon, James, et al., "The SGI Origin: A ccNUMA Highly Scalable Server", Silicon Graphics, Inc. (laudon@sgi.com) (June 1997)

EXAMINER Zhuo Li.	DATE CONSIDERED Feb. 17, 200?,

Rev 10/03 (PTO1449)

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO. 200301825-6	APPLICATION NO.	CONFIRMATION NO.
APPLICANT Luiz Andre Barroso et al.		
FILING DATE Herewith	GROUP 2186	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	5A				
	5B				
	5C				
	5D				
	5E				
	5F				
	5G				
	5H				
	5I				
	5J				
	5K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	5L					
	5M					
	5N					
	5O					
	5P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

⤳	5Q	Lenoski, Daniel et al., "The Directory-Based Cache Coherence Protcol for the DASH Multiprocessor", IEEE (1990) (CH2887-8) pp. 148-159
⤳	5R	Nayfeh, Basem A., et al., "Evaluation of Design Alternatives for a Multiprocessor Microprocessor", ACM (1996) (0-89791-786-3) pp. 67-77
⤳	5S	Nowatzyk, Andreas G., et al., "S-Connect: from Networks of Workstations to Supercomputer Performance", 22nd Annual International Symposium on Computer Architecture ("ISCA") (June 1995)

EXAMINER Zhuo Li	DATE CONSIDERED Feb. 17, 2005

Rev 10/03 (PTO1449)

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO. 200301825-6	APPLICATION NO.	CONFIRMATION NO.
APPLICANT Luiz Andre Barroso et al.		
FILING DATE Herewith	GROUP 2186	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	6A				
	6B				
	6C				
	6D				
	6E				
	6F				
	6G				
	6H				
	6I				
	6J				
	6K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	6L					
	6M					
	6N					
	6O					
	6P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	6Q	Nowatzyk, Andreas, et al., "Exploiting Parallelism in Cache Coherency Protocol Engines", Sun Microsystems Computer Corporation (August 1995)
	6R	Olukotun, Kunle, et al., "The Case of a Single-Chip Multiprocessor", Proceedings Seventh International Symposium Architectural Support for Programming Languages and Operating Systems ("ASPLOS VII") (October 1996)
	6S	Steffan, J. Gregory, et al., "The Potential for Using Thread-Level Data Speculation to Facilitate Automatic Parallelization", HPCA-4 (February 1998) pp. 1-12

EXAMINER Zhuo Li.	DATE CONSIDERED Feb. 17, 2004

Rev 10/03 (PTO1449)

FORM PTO-1449	ATTY. DOCKET NO. 200301825-6		APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Luiz Andre Barroso et al.			
	FILING DATE Herewith	GROUP 2186		

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	7A				
	7B				
	7C				
	7D				
	7E				
	7F				
	7G				
	7H				
	7I				
	7J				
	7K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	7L					
	7M					
	7N					
	7O					
	7P					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

7L	7Q	Tremblay, Marc, "MAJC-TM-5200 AVLIW Convergent MPSOC", Sun Microsystems, Inc., Microprocessor Forum (1999)
7L	7R	Kunkel, Steven, et al., "System Optimization for OLTP Workloads, IEEE (1999) (0272-1732) pp. 56-64
7L	7S	Diefendorff, Keith, "Power4 Focuses on Memory Bandwidth", Microdesign Resources, Microprocessor Report Vol. 13, No. 13, October 6, 1999

EXAMINER Zhuo Li.	DATE CONSIDERED Feb 17, 2005.

Rev 10/03 (PTO1449)

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO. 200301825-6	APPLICATION NO.	CONFIRMATION NO.
APPLICANT Luiz Andre Barroso et al.		
FILING DATE Herewith	GROUP 2186	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	8A				
	8B				
	8C				
	8D				
	8E				
	8F				
	8G				
	8H				
	8I				
	8J				
	8K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	8L					
	8M					
	8N					
	8O					
	8P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	8Q	Hammond, Lance, et al., "The Stanford Hydra CMP", Stanford University, Computer Systems Laboratory (http://www-hydra.stanford.edu) (March 2000), in EEE Micro, V.20 No. 2,
	8R	
	8S	

EXAMINER _Zhuo Li._	DATE CONSIDERED _Feb. 17, 2005._

Rev 10/03 (PTO1449)